ABSTRACT OF THE DISCLOSURE

The present invention provides a data processing apparatus and method for determining a target address for an instruction flow changing instruction. The data processing apparatus comprises a processor operable to execute a stream of instructions, and a prefetch unit operable to prefetch instructions from a memory prior to sending those instructions to the processor for execution. The prefetch unit is operable to receive from the memory simultaneously a plurality of prefetched instructions from sequential addresses in memory, and is operable to detect whether any of those prefetched instructions are an instruction flow changing instruction, and based thereon to output a fetch address for a next instruction to be prefetched by the prefecth unit. Address generation logic is also provided which is operable, for a selected prefetched instruction that is detected to be an instruction flow changing instruction, to determine a target address to be output as the fetch address. The address generation logic has a first address generation path operable to determine the target address if the selected prefetched instruction is a first prefetched instruction in the plurality, and at least one further address generation path operable to determine the target address if the selected prefetched instruction is one of the other prefetched instructions in the plurality. The first address generation path is arranged to generate the target address more quickly than the at least one other address generation path, whereby in the event that the first prefetched instruction is the selected prefetched instruction, the prefetch unit is operable to output the associated target address as the fetch address earlier than if one of the other prefetched instructions is said selected prefetched instruction.